AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A computational apparatus comprising:

a first register;

a second register;

a multiplier coupled to said first register and to said second register to provide a product of contents of said first and second registers;

a third register coupled to said multiplier to receive said product as third register contents;

~~a fourth register with its least significant bit position coupled to at least one of said third register and said first selection logic; and~~

first selection logic coupled to said first register and said third register to select register contents to be loaded into said first register; and ~~, the first selection logic to select one of the contents of said first register and the contents of said third register based on at least one of a function selection signal, a most significant bit of said third register contents, and a least significant bit of a quantity not stored in any of said first, second, and third registers~~

a fourth register with its least significant bit position coupled to at least one of said third register or said first selection logic;

wherein said first selection logic selects contents of one of the said first register and said third register based on at least one of a function selection signal, a most significant bit of said third register contents, or a least significant bit of said fourth register.

2. (Cancelled)

3. (Previously presented) The apparatus according to Claim 1, wherein said fourth register comprises a shift register having a shift selection input coupled to said function selection signal.

4. (Previously presented) The apparatus according to Claim 1, wherein said first selection logic comprises:

a first multiplexer to receive a most significant bit of said third register and a least significant bit of said fourth register, and to receive as a select input said function selection signal; and

a second multiplexer to receive an output of said first multiplexer as a select input and to receive as inputs contents of said first and third registers.

5. (Previously presented) The apparatus according to Claim 1, wherein said quantity corresponds to contents of said fourth register.

6. (Original) The apparatus according to Claim 1, further comprising:

at least one machine-accessible medium, said at least one machine-accessible medium coupled to said second register to provide at least one coefficient to load into said second register.

7. (Previously presented) The apparatus according to Claim 6, further comprising:

a second selection logic coupled between said at least one machine-accessible medium and said second register, the second selection logic to select one of at least two coefficients

provided from said at least one machine-accessible medium in response to said function selection signal.

8. (Original) The apparatus according to Claim 1, wherein said multiplier comprises a fractional unsigned multiplier.

9. (Original) The apparatus according to Claim 1, wherein said first selection logic uses one of said most significant bit of said third register and said least significant bit of said quantity based on said function selection signal.

10. (Currently amended) A system comprising:

at least one processor; and

a computational apparatus coupled to said at least one processor, said computational apparatus including:

first and second registers;

a multiplier coupled to said first and second registers to provide a product of contents of said first and second registers;

a third register coupled to said multiplier to receive said product;

~~a fourth register with its least significant bit position coupled to at least one of said third register and said selection logic; and~~

selection logic coupled to said first and third registers to select contents to load into said first register; and, ~~the selection logic adapted to select one of the contents of said first register and the contents of said third register based on at least one of a function selection signal, a most significant bit of said third register, and a least significant bit of a quantity not stored in any of said first, second, and third registers~~

a fourth register with its least significant bit position coupled to at least one of said third register and said selection logic,

wherein the selection logic is adapted to select one of the contents of said first register and the contents of said third register based on at least one of a function selection signal, a most significant bit of said third register contents, or a least significant bit of said fourth register.

11. (Original) The system according to Claim 10, wherein said at least one processor is adapted to furnish at least one of an operand and said function selection signal to said computational apparatus.

12. (Original) The system according to Claim 10, further comprising:

at least one memory coupled to at least one of said at least one processor and said computational apparatus.

13. (Cancelled)

14. (Previously presented) The system according to Claim 10, wherein said fourth register is adapted to be initialized to at least one of an operand and a portion of a result, in accordance with said function selection signal.

15. (Previously presented) The system according to Claim 10, wherein said quantity corresponds to contents of said fourth register.

16. (Original) The system according to Claim 10, wherein said first register is

adapted to be initialized to at least one of an operand and an initial value for at least part of a result, in accordance with said function selection signal.

17. (Original) The system according to Claim 10, wherein said second register is adapted to be loaded with a coefficient chosen according to said function selection signal.

18. (Currently amended) A method, comprising:

loading a first operand into a first register;

loading a second operand into a second register;

computing a product of said first and second operands using a multiplier;

~~loading said first register with one of said product and said first operand as a new first operand, based at least in part on one of a function selection signal, a most significant bit of said product, and a least significant bit of a third operand;~~

loading said product into a third register; ~~and~~

loading said third operand into a fourth register with its least significant bit position coupled to at least one of said third register and said function selection signal; and

loading said first register with one of said product and said first operand as a new first operand, based at least in part on one of a function selection signal, a most significant bit of said product, or a least significant bit of the fourth register.

19. (Cancelled)

20. (Previously presented) The method according to Claim 18, wherein said third operand comprises one of at least a partial result of a desired computation and at least part of an operand on which to perform a desired computation; and

wherein said first operand comprises one of at least part of an operand on which to perform a desired computation and an initial value of at least part of a result of a desired computation.

21. (Withdrawn) An apparatus, comprising:

a first register;

a second register;

selection logic coupled to said second register and to provide an output in response to a select input, said selection logic also coupled to a constant input value, the select input to select between a coefficient and said constant input value; and

a multiplier coupled to said first register and to said output of said selection logic to provide a product of contents of said first register and said output of said selection logic;

wherein said multiplier is further coupled to said first register to provide said product as an input to said first register.

22. (Withdrawn) The apparatus according to Claim 21, wherein said coefficient is provided to said selection logic by said second register.

23. (Withdrawn) The apparatus according to Claim 21, wherein one of said coefficient and said constant input value is provided by said selection logic to said second register to be second register contents, and wherein said second register contents are provided to said multiplier.

24. (Withdrawn) The apparatus according to Claim 21, further comprising:

a third register coupled to said multiplier to receive said product and to said first

register to provide said product.

25. (Withdrawn) The apparatus according to Claim 21, further comprising:

a fourth register adapted to receive an operand and to provide a least significant bit of said operand to said select input of said selection logic.

26. (Withdrawn) The apparatus according to Claim 21, wherein said selection logic comprises a multiplexer.

27. (Withdrawn) The apparatus according to Claim 21, wherein said multiplier comprises a fractional unsigned multiplier.

28. (Withdrawn) A method, comprising:

loading a first operand into a first register;

selecting a second operand from one of an iteration-specific coefficient and a constant input value based on a least significant bit of a third operand;

computing a product of said first and second operands; and

replacing said first operand with said product in preparation for a next iteration of said method.

29. (Withdrawn) The method according to Claim 28, further comprising:

loading said third operand into a second register.

30. (Withdrawn) The method according to Claim 29, wherein said loading said third operand comprises:

initializing said third operand to a non-integer portion of a number on which to operate.

31. (Withdrawn) A system comprising:

at least one processor; and

a computational apparatus coupled to said at least one processor, said computational apparatus including:

first and second registers;

selection logic coupled to said second register to provide an output in response to a select input, said selection logic also coupled to a constant input value, the select input to select between a coefficient and said constant input value; and

a multiplier coupled to said first register and to said output of said selection logic to provide a product of contents of said first register and said output of said selection logic, wherein said multiplier is further coupled to said first register to provide said product as an input to said first register.

32. (Withdrawn) The system according to Claim 31, further comprising:

at least one memory coupled to at least one of said at least one processor and said computational apparatus.

33. (Withdrawn) The system according to Claim 31, said computational apparatus further comprising:

a third register coupled to said multiplier to receive said product and to said first register to provide said product.

34. (Withdrawn) The system according to Claim 31, said computational apparatus further comprising:

a fourth register with its least significant bit position coupled to said selection logic, said fourth register adapted to be initialized to at least a portion of an operand.

35. (Withdrawn) The system according to Claim 31, wherein said coefficient is provided to said selection logic by said second register.

36. (Withdrawn) The system according to Claim 31, wherein one of said coefficient and said constant input value is provided by said selection logic to said second register to be second register contents, and wherein said second register contents are provided to said multiplier.

37. (Withdrawn) The system according to Claim 31, wherein said selection logic comprises a multiplexer.

38. (Withdrawn) The system according to Claim 31, wherein said multiplier comprises a fractional unsigned multiplier.